GSM 3 V Transceiver IF Subsystem

AD6432

FEATURES

Fully Compliant with Standard and Enhanced GSM Specification
- **DC-350 MHz RF Bandwidths**
- **80 dB Gain Control Range**
- **I/Q Modulation and Demodulation**
- **Onboard Phase Locked Tunable Oscillator**
- **On-Chip Noise Roofing IF Filters**

Ultralow Power Design
- **2.7 V–3.6 V Operating Voltage**
- **User-Selectable Power-Down Modes**

Small 44-Lead TQFP Package

Interfaces Directly with AD20msp410 and AD20msp415 GSM Baseband Chipsets

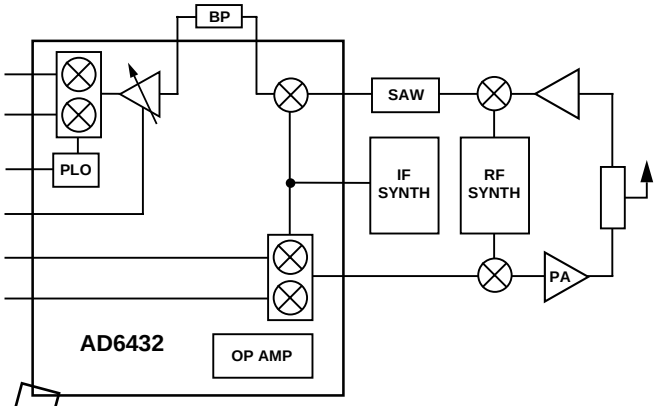
APPLICATIONS

I/Q Modulated Digital Wireless Systems

GSM Mobile Radios

GSM PCMCIA Cards

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD6432 IF IC provides the complete transmit and receive IF signal processing, including I/Q modulation and demodulation, necessary to implement a digital wireless transceiver such as a GSM handset. The AD6432 may also be used for other wireless TDMA standards using I/Q modulation.

The AD6432's receive signal path is based on the proven architecture of the AD607 and the AD6459. It consists of a mixer, gain-controlled amplifiers, integrated roofing filter and I/Q demodulators based on a PLL. The low noise, high-intercept variable-gain mixer is a doubly-balanced Gilbert-cell type. It has a nominal –13 dBm input-referred 1 dB compression point and a 0 dBm input-referred third-order intercept.

The gain-control input accepts an external control voltage input from an external AGC detector or a DAC. It provides an 80 dB gain range with 27.5 mV/dB gain scaling, where the mixer and the IF gains vary together.

The I and Q demodulators provide inphase and quadrature baseband outputs to interface with Analog Devices' AD7015 and AD6421 (GSM, DCS1800, PCS1900) baseband converters. An onboard quadrature VCO, externally phase-locked to the IF signal, drives the I and Q demodulators. The quadrature phase-locked oscillator (QPLO) requires no external components for frequency control or quadrature generation, and demodulates signals at standard GSM system IFs of 13 MHz, or 26 MHz with a reference input frequency of 13 MHz; or, in general, 1X or 2X the reference frequency. Maximum reference frequency is 25 MHz.

This reference signal is normally provided by an external VCTCXO under the control of the radio's digital signal processor. The transmit path consists of an I/Q modulator and buffer amplifier, suitable for carrier frequencies up to 300 MHz and provides an output power of –17.5 dBm in a 50 Ω system. The quadrature LO signals driving the I and Q modulator are generated internally by dividing by two the frequency of the signal presented at the differential LO port of the AD6432. In both the transmit and receive paths, onboard filters provide 30 dB of stopband attenuation.

The AD6432 comes in a 44-lead plastic thin quad flatpack (TQFP) surface mount package.

REV. 0

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AD6432–SPECIFICATIONS (T_A = +25°C, V_P = 3.0 V, GREF = 1.25 V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
RX RF MIXER					
RF Input Frequency				350	MHz
AGC Conversion Gain Variation	Z_{IN} = 150 Ω: 0.2 V < V_{GAIN} < 2.4 V		–3 to +15		dB
Input 1 dB Compression Point	At V_{GAIN} = 2.4 V, Z_{IN} = 150 Ω		–13		dBm
Input Third-Order Intercept	At V_{GAIN} = 0.2 V, RF_{IN} = –25 dBm		0		dBm
SSB Noise Figure	At Z_{IN} = 150 Ω, F_{RF} = 246 MHz, F_{LO} = 272 MHz, V_{GAIN} = 0.2 V		10		dB
RX IF AMPLIFIER					
AGC Gain Variation	0.2 V < V_{GAIN} < 2.4 V		–14 to 48		dB
Input Resistance	at V_{GAIN} = 0.2 V		5		kΩ
Operating Frequency Range		10		50	MHz
GAIN CONTROL					
Total Gain Control Range	Mixer+IF+Demod, 0.2 V < V_{GAIN} < 2.4 V		80		dB
Control Voltage Range at GAIN		0.2		2.4	V
Gain Scaling			27.5		mV/dB
Gain Law Conformance			±0.1		dB
Bias Current at GREF			–0.5		µA
Input Resistance at Gain			20		kΩ
INTEGRATED IF FILTER					
BPF Center Frequency	f_{REF} = 13 MHz				
IFS0 = 1	"0" = Connect to Ground, "1" = Connect to V_P		13		MHz
IFS0 = 0	"0" = Connect to Ground, "1" = Connect to V_P		26		MHz
BPF –3 dB BW	f_{REF} = 13 MHz				
IFS0 = 1	"0" = Connect to Ground, "1" = Connect to V_P		5		MHz
IFS0 = 0	"0" = Connect to Ground, "1" = Connect to V_P		10		MHz
I AND Q DEMODULATOR					
Demodulation Gain			17		dB
Output Voltage Range	Differential	0.3		V_{POS} – 0.2	V
Output Voltage Common-Mode Level	Not Power Supply Independent		1.5		V
Output Offset Voltage	Differential, V_{GAIN} = GREF	–150		+150	mV
Error in Quadrature	Differential from I to Q, IF = 13 MHz		1	3.5	Degrees
Amplitude Match			0.25		dB
I/Q Output BW	C_{LOAD} = 10 pF		3		MHz
Output Resistance	Each Pin		4.7		kΩ
QUADRATURE IF PLL					
Operating Frequency Range		10		50	MHz
Reference Frequency Voltage Level			200		mV p-p
Reference Frequency Range				25	MHz
Acquisition Time	Using 1 kΩ, 1 nF Loop Filter		80		µs
TRANSMIT MODULATOR					
Carrier Output Frequency				300	MHz
Output Power	R_{LOAD} = 150 Ω, Power at Final 50 Ω, F_{IF} = 272 MHz		–17.5		dBm
Input 1 dB Compression Point	R_{LOAD} = 150 Ω (Differential)		14		dBm
I/Q Input Signal Amplitude	Differential		2.056		V p-p
I/Q Input Signal Required DC Bias			1.2		V
I/Q Input BW			1		MHz
I/Q Input Resistance		100			kΩ
I/Q Phase Balance	With LOs 2nd Harmonic 30 dBc Bellow Fundamental		±1.5		Degrees
I/Q Amplitude Balance	With LOs 2nd Harmonic 30 dBc Bellow Fundamental		±0.1		dB
Output Harmonic Content	R_{LOAD} = 150 Ω		–45 (3rd)		dBc
			–65 (5th)		dBc
Carrier Feedthrough	$F_{CARRIER}$ = 272 MHz		–33		dBc
Sideband Suppression	I and Q Inputs Driven In Quadrature		–37		dBc

Parameter	Conditions	Min	Typ	Max	Units
LO PORT (LOLO and LOHI)					
Input Frequency		200		600	MHz
Input Signal Voltage Range	Differential	200			mV p-p
Input Resistance	Input Pull-Up Resistors to V_{POS} (Each Pin)		500		Ω
AUXILIARY OP AMPLIFIER					
Small Signal –3 dB Bandwidth			50		MHz
Input Signal Voltage Range		0.1		V_{POS} – 2.1	V
Input Offset Voltage			±4		mV
Input Bias Current			–150		nA
Output Signal Voltage Range	With R_{LOAD} > 4 kΩ	0.1		V_{POS} – 0.2	V
POWER CONSUMPTION					
Supply Voltage		2.7	3	3.6	V
Transmit Mode			13		mA
Receive Mode	At V_{GAIN} = 1.2 V		13		mA
Sleep Mode			< 5		µA
OPERATING TEMPERATURE RANGE		–25		+85	°C

NOTES
All reference to dBm is relative to 50 Ω.

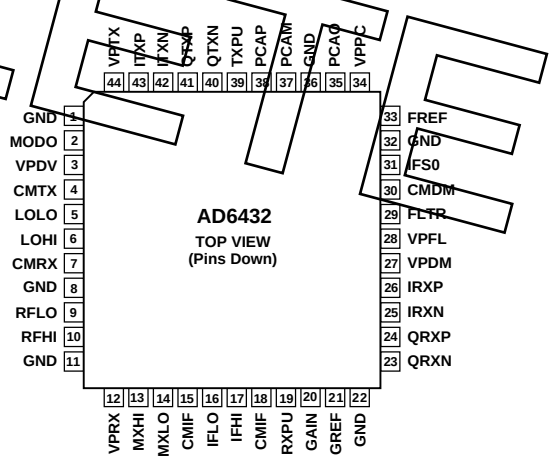
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPDV, VPPX, VPDM, VPFL, VPPC, VPRX, to CMTX, CMRX, CMIF, CMD . . . . . +3.6 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . –25°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering (60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics: 44-lead TQFP package: θ_{JA} = 126°C.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD6432AST	–25°C to +85°C	44-Pin Plastic TQFP	ST-44

*ST = Thin Quad Flatpack.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6432 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Label	Description	Function
1	GND	PCB Ground	Not Bonded to IC
2	MODO	TX Modulator Output	AC Coupled, Drives 150 Ω into 50 Ω
3	VPDV	LO2 Divided by 2 Supply Voltage	V_{POS}
4	CMTX	On-Chip TX Mixer Common	Ground
5	LOLO	Differential RX Mixer LO2 Input Negative	AC Coupled, V_{POS} to V_{POS} – 100 mV
6	LOHI	Differential RX Mixer LO2 Input Positive	AC Coupled, V_{POS} – 100 mV to V_{POS}
7	CMRX	On-Chip RX Mixer Common	Ground
8	GND	PCB Ground	Not Bonded to IC
9	RFLO	Differential RX Mixer IF1 Input Negative	AC Coupled
10	RFHI	Differential RX Mixer IF1 Input Positive	AC Coupled
11	GND	PCB Ground	Not Bonded to IC
12	VPRX	RX Section Supply Voltage	V_{POS}
13	MXHI	Differential RX IF1/IF2 Mixer Output Positive	See Figure 30
14	MXLO	Differential RX IF1/IF2 Mixer Output Negative	See Figure 30
15	CMIF	On-Chip RX IF2 Common	Ground
16	IFLO	Differential RX IF2 Input Negative	AC Coupled
17	IFHI	Differential RX IF2 Input Positive	AC Coupled
18	CMIF	On-Chip RX IF2 Common	Ground
19	RXPU	RX Enable (Power-Up)	Off = Low < 0.6 V, On = High > 2.5 V
20	GAIN	RX VGA Gain Control Input	0.2 V–2.4 V Using 3 V Supply. Max Gain at 0.2 V
21	GREF	RX VGA Reference Voltage	1.2 V typ
22	GND	PCB Ground	Not Bonded to IC
23	QRXN	Differential Demodulator Q Output Negative	Internal 4.7 kΩ Resistor in Series with the Output
24	QRXP	Differential Demodulator Q Output Positive	Internal 4.7 kΩ Resistor in Series with the Output
25	IRXN	Differential Demodulator I Output Negative	Internal 4.7 kΩ Resistor in Series with the Output
26	IRXP	Differential Demodulator I Output Positive	Internal 4.7 kΩ Resistor in Series with the Output
27	VPDM	Demodulator Supply Voltage	V_{POS}
28	VPFL	I/Q LO PLL Filter Cap. Supply Voltage	To V_{POS} with Good Decoupling
29	FLTR	I/Q LO PLL Filter	Referenced to VPFL
30	CMDM	On-Chip Demodulator Common	Ground
31	IFS0	IF2 Frequency Select Bit	"0" = Low < 0.6 V, "1" = High > 2.5 V
32	GND	PCB Ground	Not Bonded to IC
33	FREF	Reference Input (13 MHz for GSM)	AC Coupled. Use 200 mV p-p Input Signal
34	VPPC	Auxiliary Op Amp Supply Voltage	V_{POS}
35	PCAO	Auxiliary Op Amp Output	Active when TXPU Is High
36	GND	PCB Ground	Not Bonded to IC
37	PCAM	Differential Auxiliary Op Amp Input Negative	0.1 V to V_{POS} – 2.1 V
38	PCAP	Differential Auxiliary Op Amp Input Positive	0.1 V to V_{POS} – 2.1 V
39	TXPU	TX Enable (Power-Up)	Low < 0.6 V, High > 2.5 V
40	QTXN	Differential Modulator Q Input Negative	DC Coupled, 1.2 V ± 514 mV
41	QTXP	Differential Modulator Q Input Positive	DC Coupled, 1.2 V ± 514 mV
42	ITXN	Differential Modulator I Input Negative	DC Coupled, 1.2 V ± 514 mV
43	ITXP	Differential Modulator I Input Positive	DC Coupled, 1.2 V ± 514 mV
44	VPTX	TX Section Supply Voltage	V_{POS}

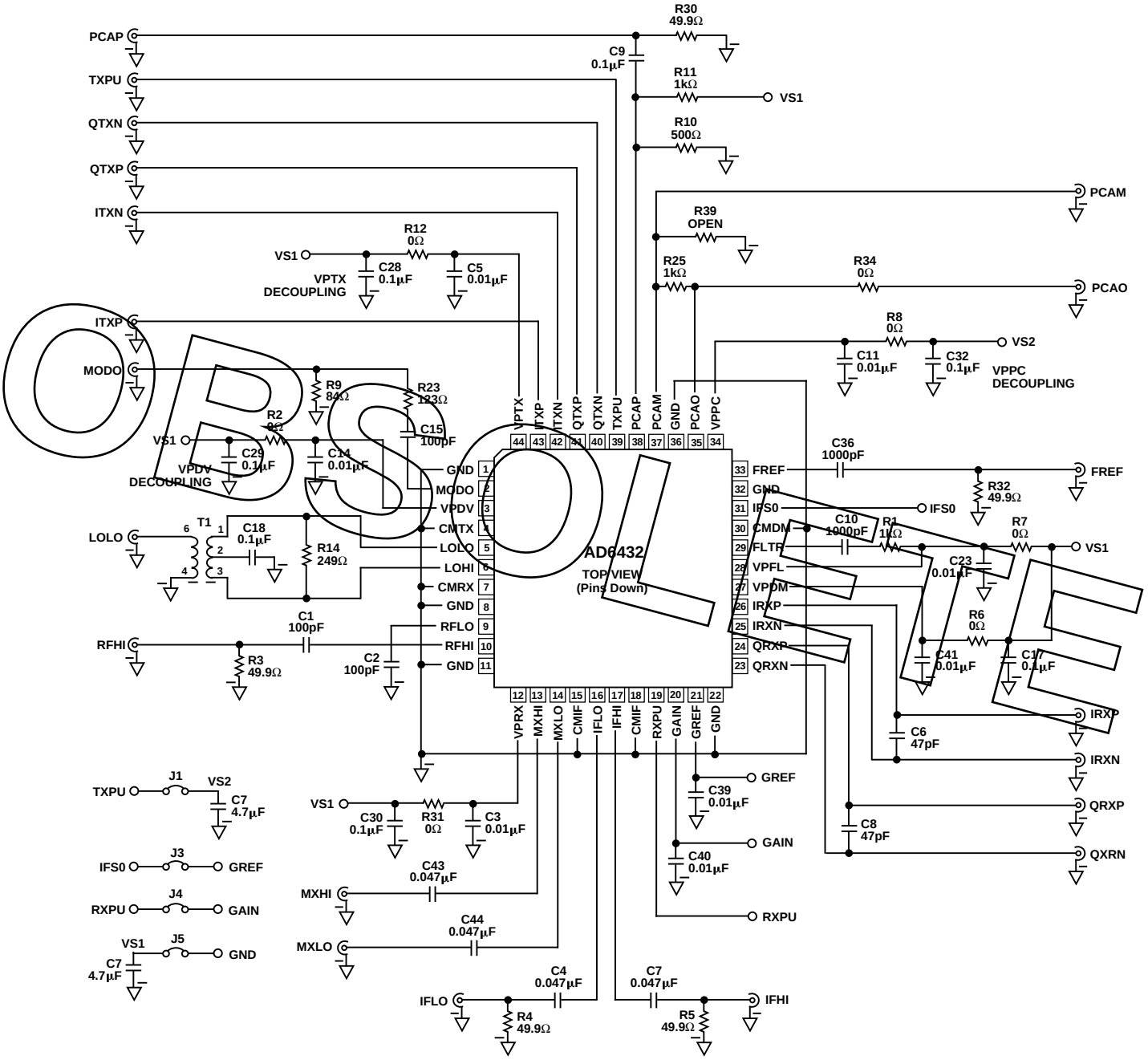
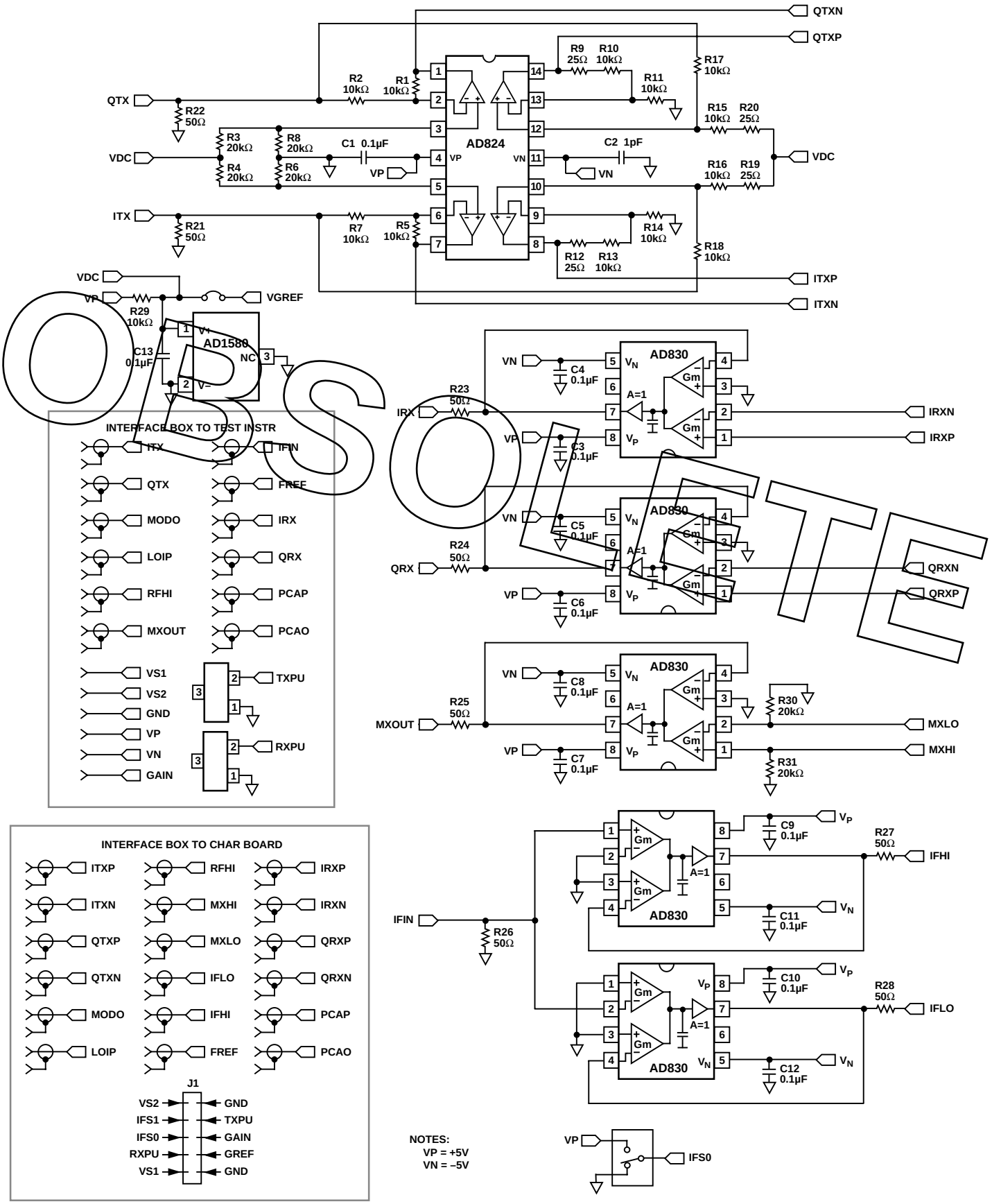


Figure 1. Characterization Board



OBSOLETE

Figure 2. Characterization Test Set

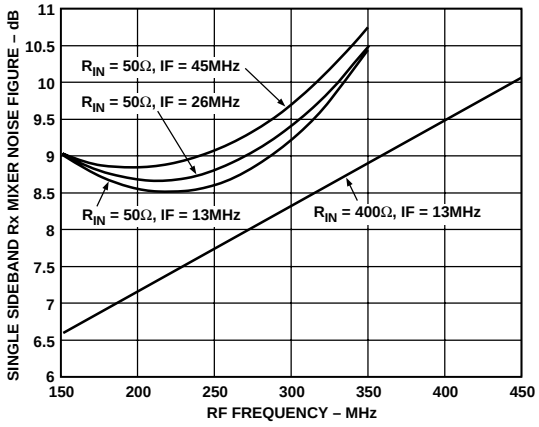


Figure 3. Rx Mixer Noise Figure vs. RF Frequency, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V, V_{GAIN} = 0.2 V

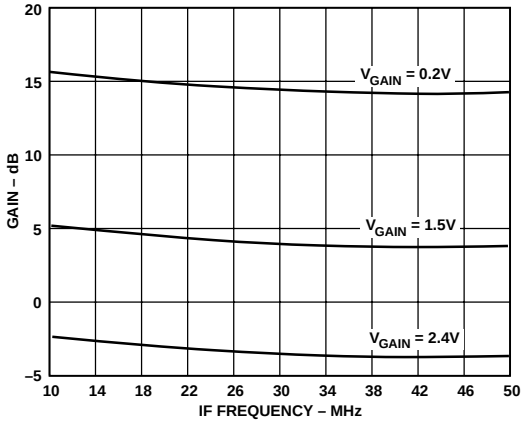


Figure 6. Mixer Conversion Gain vs. IF Frequency, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V, F_{RF} = 250 MHz

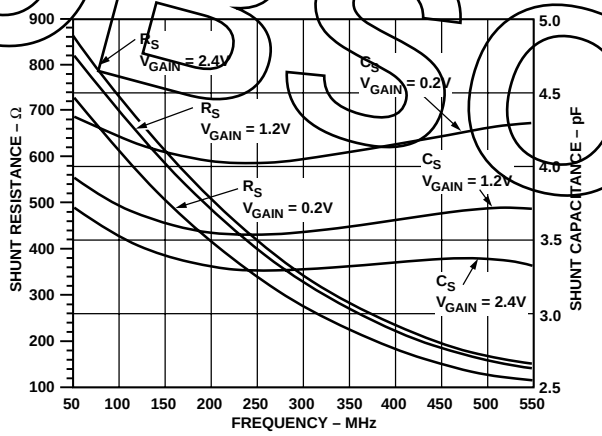


Figure 4. Rx Mixer Input Impedance vs. RF Frequency, V_{POS} = 3 V, T_A = +25°C, V_{GREF} = 1.2 V

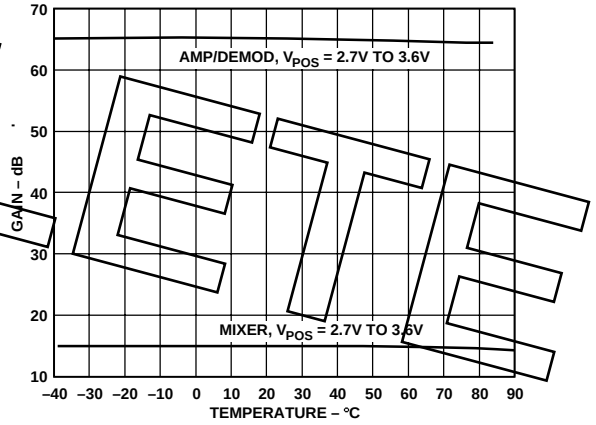


Figure 7. Rx Mixer Conversion Gain and IF Amplifier/ Demodulator Gain vs. Temperature, V_{GAIN} = 0.2 V, V_{GREF} = 1.2 V, F_{IF} = 26 MHz, F_{RF} = 250 MHz

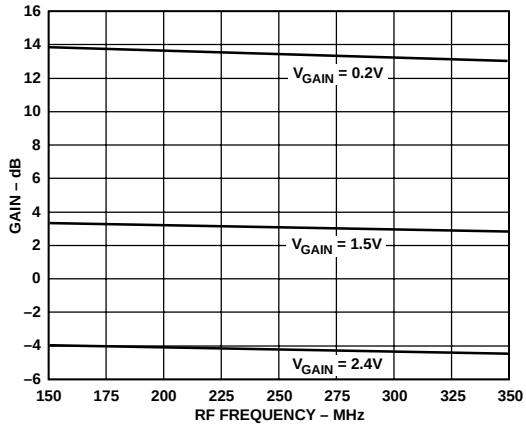


Figure 5. Rx Mixer Conversion Gain vs. RF Frequency, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V, F_{IF} = 26 MHz

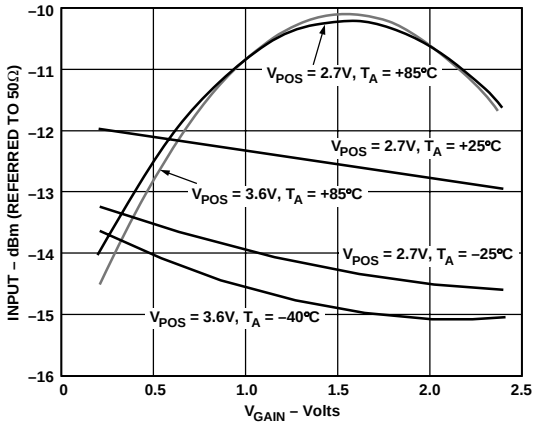


Figure 8. Rx Mixer Input 1 dB Compression Point vs. V_{GAIN}, V_{GREF} = 1.2 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz

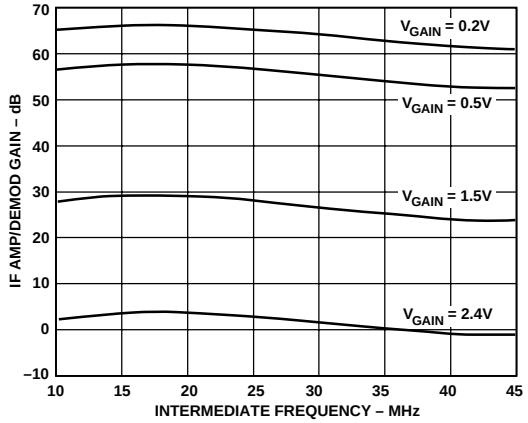


Figure 9. IF Amplifier and Demodulator Gain vs. IF Frequency, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V

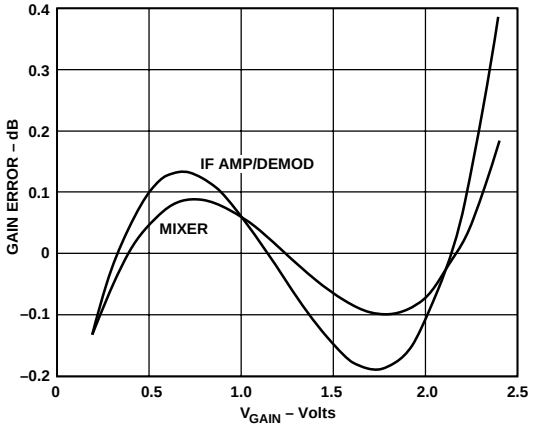


Figure 12. Gain Error vs. Gain Control Voltage, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz

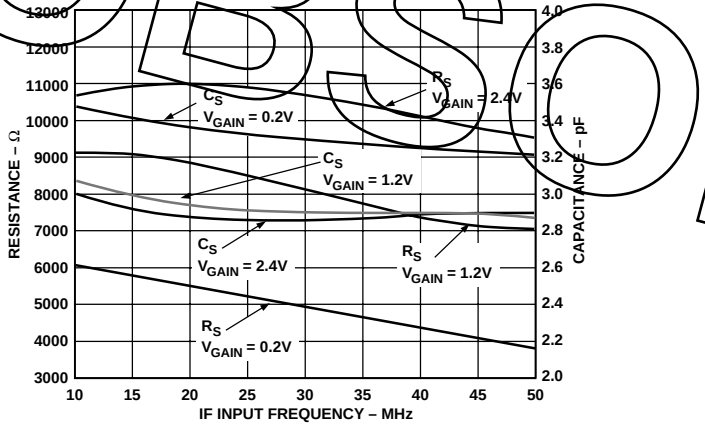


Figure 10. IF Amplifier Input Impedance vs. Frequency, T_A = +25°C, V_{POS} = 3 V, V_{GREF} = 1.2 V

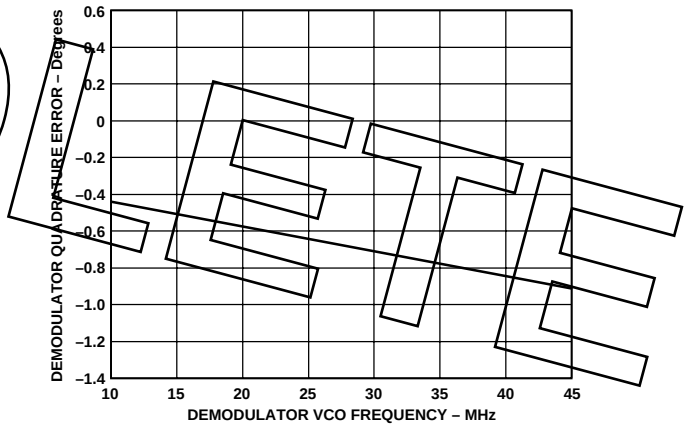


Figure 13. Demodulator Quadrature Error vs. FREF Frequency, T_A = +25°C, V_{POS} = 3 V

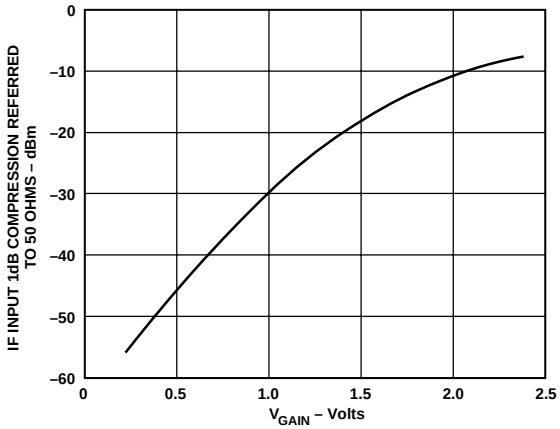


Figure 11. IF Amplifier/Demodulator Input 1 dB Compression Point vs. V_{GAIN} , F_{IF} = 26 MHz, V_{GREF} = 1.2 V, T_A = +25°C, V_{POS} = 3 V

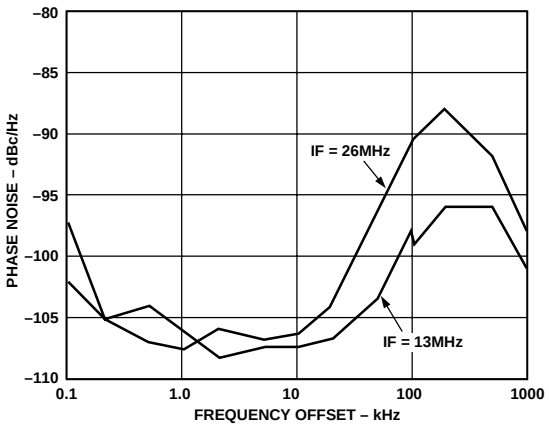


Figure 14. PLL Phase Noise vs. Frequency, V_{POS} = 3 V, C_{FLTR} =1 nF, R_{FLTR} =1 kΩ, FREF = 13 MHz

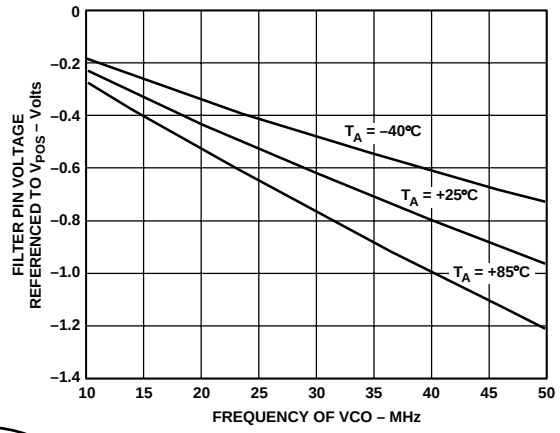


Figure 15. PLL Loop Voltage at FLTR Pin (KVCO) vs. Frequency

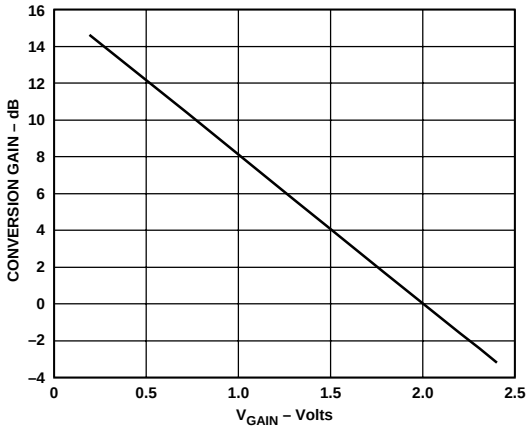


Figure 18. Rx Mixer Conversion Gain vs V_{GAIN}, T_A = +25°C, V_{POS} = 3 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz, V_{GREF} = 1.2 V

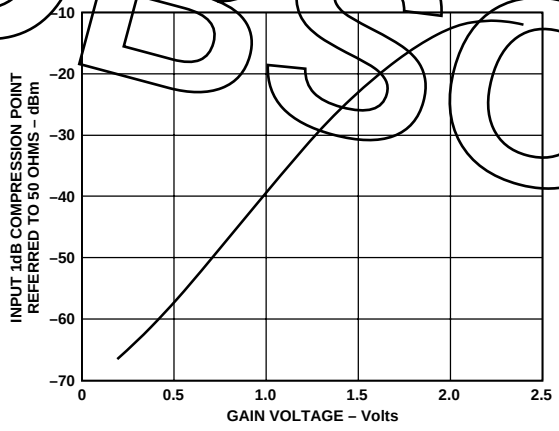


Figure 16. System (Mixer + IF LC Filter + IF Amplifier + Demodulator) 1 dB Compression Point vs. V_{GAIN}, T_A = +25°C, V_{POS} = 3 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz, V_{GREF} = 1.2 V

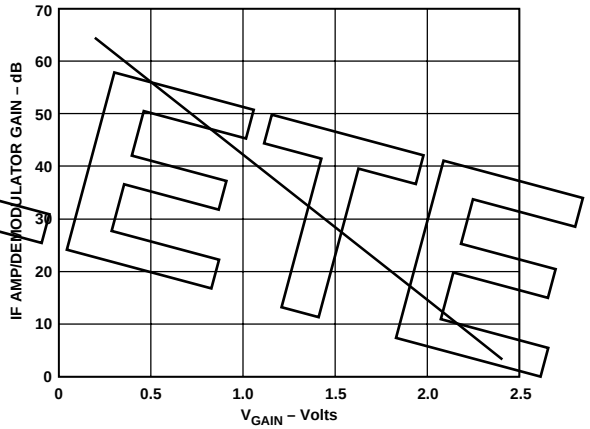


Figure 19. IF Amplifier/Demodulator Gain vs. V_{GAIN}, T_A = +25°C, V_{POS} = 3 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz, V_{GREF} = 1.2 V

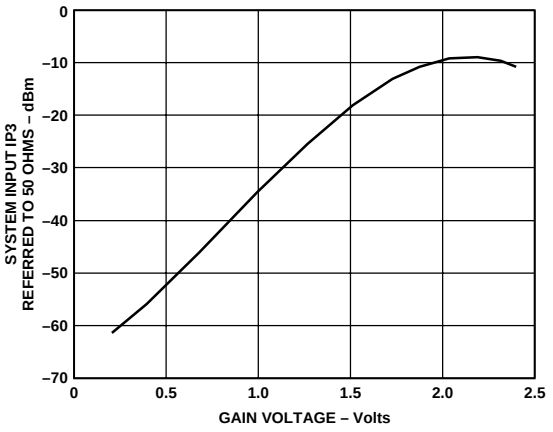


Figure 17. System (Mixer + IF LC Filter + IF Amplifier + Demodulator) IP3 vs. V_{GAIN}, T_A = +25°C, V_{POS} = 3 V, F_{IF} = 26 MHz, F_{RF} = 250 MHz, V_{GREF} = 1.2 V

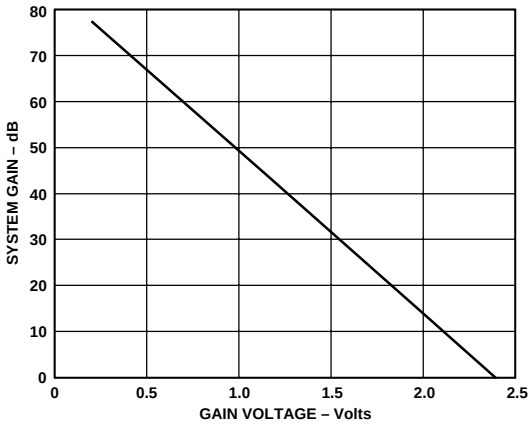


Figure 20. System (Mixer + IF LC Filter + IF Amplifier + Demodulator) Gain vs. V_{GAIN}, T_A = +25°C, V_{POS} = 3 V, F_{IF} =26 MHz, F_{RF} = 250 MHz, V_{GREF} = 1.2 V

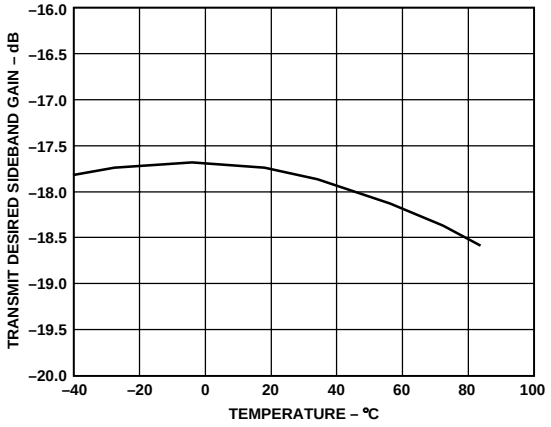


Figure 21. Tx Desired Sideband Gain vs. Temperature, T_A = +25°C, V_{POS} = 3 V, $F_{CARRIER}$ = 280 MHz, I and Q Inputs Driven in Quadrature

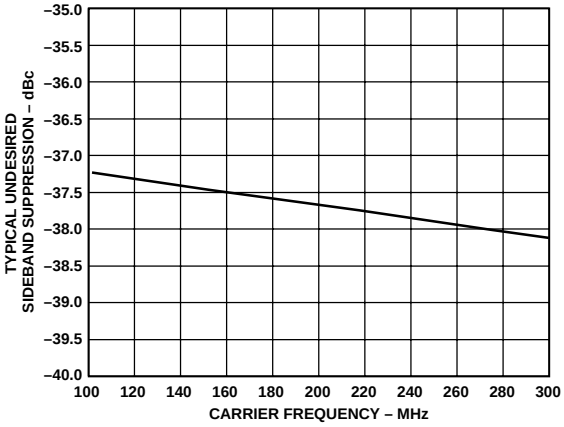


Figure 24. Tx Typical Undesired Sideband Suppression vs. $F_{CARRIER}$, T_A = +25°C, V_{POS} = 3 V

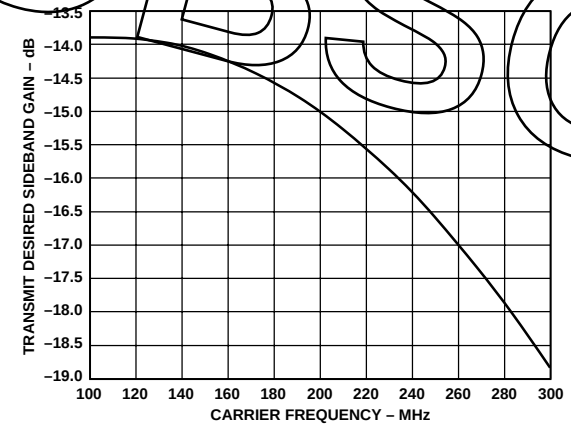


Figure 22. Tx Desired Sideband Gain vs. $F_{CARRIER}$, T_A = +25°C, V_{POS} = 3 V

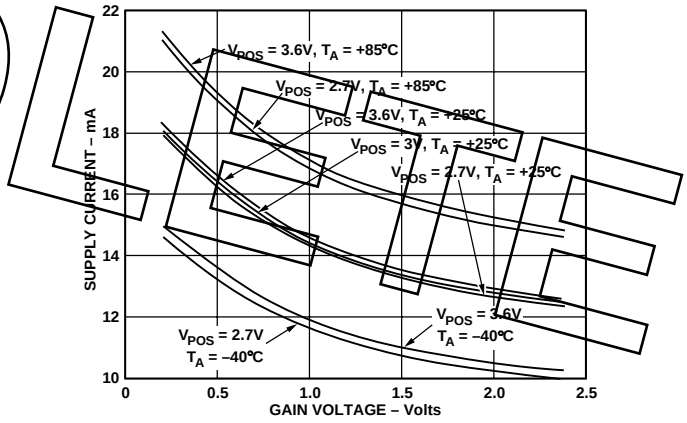


Figure 25. Rx Mode Supply Current vs. V_{GAIN}, V_{GREF} = 1.2 V

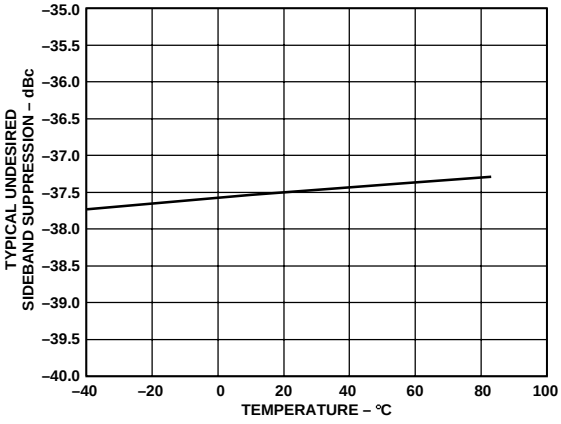


Figure 23. Tx Typical Undesired Sideband Suppression vs. Temperature, T_A = +25°C, V_{POS} = 3 V

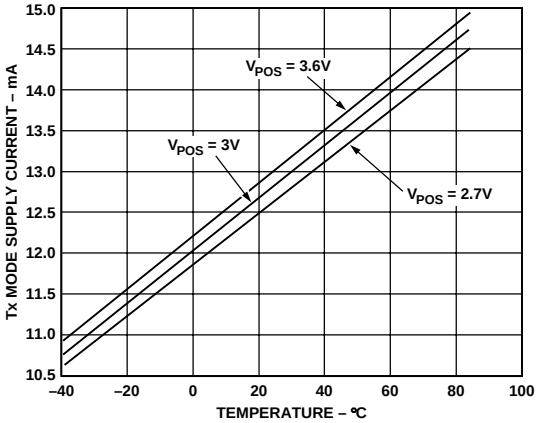


Figure 26. Tx Mode Supply Current vs. Temperature

PRODUCT OVERVIEW

The AD6432 provides most of the active circuitry required to realize a complete low power, single-conversion superheterodyne time division transceiver, or the latter part of a double-conversion transceiver, at input receive frequencies up to 350 MHz with an IF from 10 MHz to 50 MHz and transmit frequencies up to 300 MHz. The internal I/Q demodulators, with their associated phase-locked loop and the internal I/Q modulator, support a wide variety of modulation modes, including n-PSK, n-QAM, and GMSK. A single positive supply voltage of 3 V is required (2.7 V minimum, 3.6 V maximum) at a typical supply current of 13 mA at midgain in receive mode and 13 mA in transmit mode. In the following discussion, V_{POS} will be used to denote the power supply voltage, which will be assumed to be 3 V.

Figure 27 shows the main sections of the AD6432. In the receive path, it consists of a variable-gain UHF mixer and linear two-stage IF strip, both of which together provide a calibrated voltage-controlled gain range of more than 80 dB, followed by a tunable IF bandpass filter and dual quadrature demodulators. These are driven by inphase and quadrature clocks generated by a Phase-Locked Loop (PLL) locked to a corrected external reference. In the transmit path it consists of a quadrature modulator followed by a low-pass filter. The quadrature modulator is driven by quadrature frequencies that are generated internally by dividing the external local oscillator frequency by two. A CMOS-compatible power-down interface completes the AD6432.

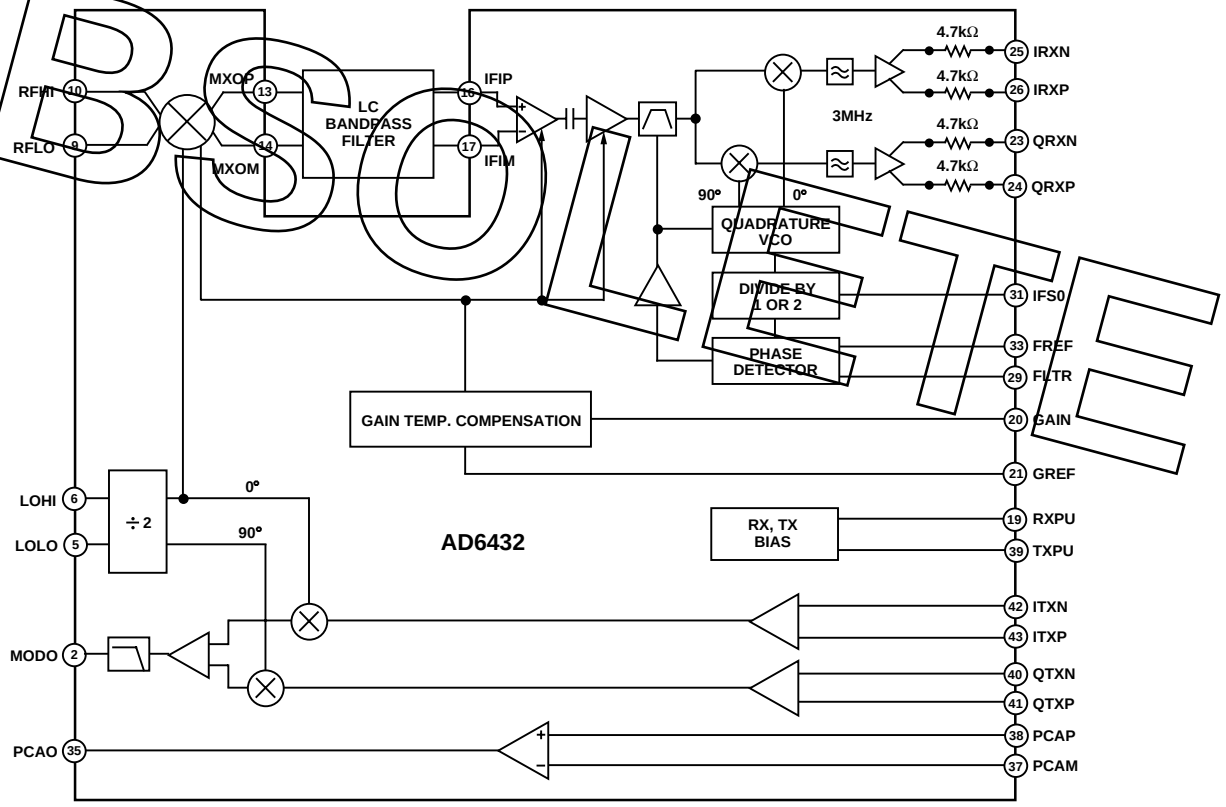


Figure 27. Functional Block Diagram

Receive Mixer

The UHF mixer is an improved Gilbert-cell design that can operate from low frequencies (it is internally dc-coupled) up to an RF input of 350 MHz. The dynamic range at the input of the mixer is determined, at the upper end, by the maximum input signal level of ±71 mV (–13 dBm in 50 Ω between RFHI and RFLO) up to which the mixer remains linear and, at the lower end, by the noise level. It is customary to define the linearity of a mixer in terms of the 1 dB gain-compression point and third-order intercept, which for the AD6432 are –13 dBm and 0 dBm, respectively, in a 50 Ω system.

The mixer's RF input port is differential, that is, pin RFLO is functionally identical to RFHI, and these nodes are internally biased. The RF port can be modeled as a parallel RC circuit as shown in Figure 29. The local oscillator input of the receive mixer is internally provided by the LO divided by two.

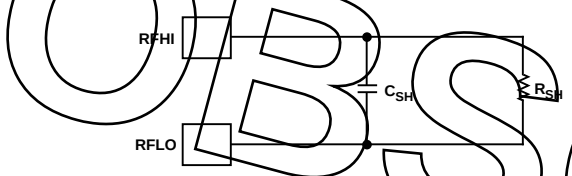


Figure 28. Mixer Port Modeled as a Parallel RC Network At V_{GAIN} = 1.2 V and F_{RF} = 250 MHz, C_{SH} = 3.5 pF and R_{SH} = 400 Ω (See Figure 4)

The output of the mixer is differential. The nominal conversion gain is specified for operation into a 26 MHz LC IF bandpass filter, as shown in Figure 29 and Table I.

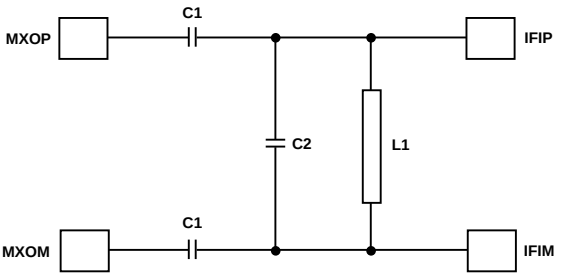


Figure 29. Suggested IF Filter Inserted Between the Mixer's Output Port and the Amplifier's Input Port

The conversion gain is measured between the mixer input and the input of this filter, and varies between –3 dB and +15 dB.

Table I. Filter Component Values for Selected Frequencies

Frequency	C1	L1	C2
13 MHz	27 pF	0.82 µH	180 pF
26 MHz	22 pF	0.39 µH	82 pF

The maximum permissible signal level between MXOP and MXOM is determined by the maximum gain control voltage. The mixer output port, having pull-up resistors of 250 Ω to VPRX, is shown in Figure 30.

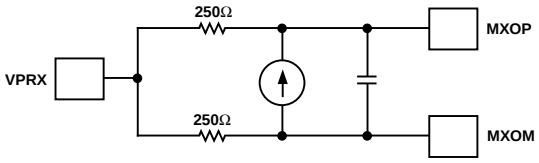


Figure 30. Mixer Output Port

IF Amplifier

Most of the gain in the AD6432 receive section is provided by the IF amplifier strip, which comprises two stages. Both are fully differential and each has a gain span of 31 dB for the AGC voltage range of 0.2 V to 2.4 V. Thus, in conjunction with the variable gain of the mixer, the total gain span is 80 dB. The overall IF gain varies from –14 dB to +48 dB for the nominal AGC voltage of 0.2 V to 2.4 V. Maximum gain is at V_{GAIN} = 0.2 V.

The IF input is differential, at IFHI and IFLO. Figure 32 shows a simplified schematic of the IF interface modeled as parallel RC network.

The operative range of the IF amplifier is approximately 50 MHz from IFHI and IFLO through the demodulator.

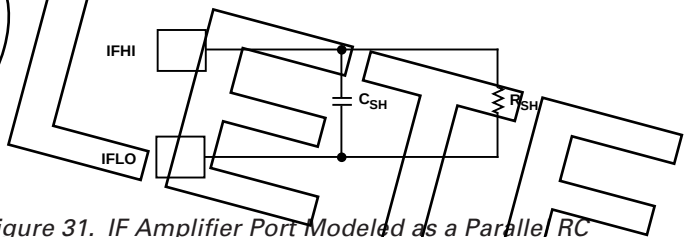


Figure 31. IF Amplifier Port Modeled as a Parallel RC Network for V_{GAIN} = 1.2 V and F_{IF} = 26 MHz, C_{SH} = 3 pF, R_{SH} = 8.5 kΩ (See Figure 10)

Gain Scaling

The overall gain of the AD6432, expressed in decibels, is linear with respect to the AGC voltage V_{GAIN} at Pin GAIN. The gain of all sections is maximum when V_{GAIN} is 0.2, and falls off as the bias is increased to V_{GAIN} = 2.4 V and is independent of the power supply voltage. The gain of all stages changes simultaneously. The AD6432's gain scaling is also temperature-compensated. Note that GAIN pin of the AD6432 is an input driven by an external low impedance voltage source, normally a DAC, under the control of radio's digital processor.

The gain-control scaling is directly proportional to the reference voltage applied to the Pin GREF and is independent of the power supply voltage. When this input is set to the nominal value of 1.2 V, the scale is nominally 27.5 mV/dB (36.4 dB/V). Under these conditions, 80 dB of gain range (mixer plus IF) corresponds to a control voltage of 0.2 V < = V_G < = 2.4 V. The final centering of this 2.2 V range depends on the insertion losses of the IF filters used.

Pin GREF can be tied to an external voltage reference, V_{REF}, provided, for example, by a AD1580 (1.21 V) voltage reference.

When using the Analog Devices AD7013 (IS54, TETRA and satellite receiver applications) and AD7015 or AD6421 (GSM, DCS1800, PCS1900) baseband converters, the external reference may also be provided by the reference output of the

baseband converters. The interface between the AD6432 and the AD6421 baseband converter is shown in Figure 35. The AD7015 baseband converter provides a V_R of 1.23 V; an auxiliary DAC in the AD7015 can be used to generate the AGC voltage. Since it uses the same reference voltage, the numerical input to this DAC provides an accurate RSSI value in digital form, no longer requiring the reference voltage to have high absolute accuracy.

Tunable Filter and I/Q Demodulators

The demodulators (I and Q) receive their inputs internally from the IF amplifier through a two-pole tunable-frequency bandpass filter. This filter is centered on the IF frequency and its bandwidth is approximately equal to forty per cent of the IF frequency. The filter attenuates the amount of noise present at the input of the demodulators.

Each demodulator comprises a full-wave synchronous detector followed by a 3 MHz, two-pole low-pass filter, producing differential outputs at pins IRXP and IRXN, and QRXP and QRXN. Using the I and Q demodulators for IFs above 50 MHz is precluded by the 10 MHz to 50 MHz range of the PLL used in the Demodulator section.

The I and Q outputs are differential and can swing up to 2 V p-p at the low supply voltage of 2.7 V. They are nominally centered at 1.5 V independent of power supply. They can therefore directly drive the receive ADCs in the AD7015 or AD6421 baseband converters, which require an amplitude of 1.23 V to fully load them when driven by a differential signal. The conversion gain of the I and Q demodulators is 17 dB.

A simple 1-pole RC filter at the I and Q outputs, with its corner above the modulation bandwidth is sufficient to attenuate undesired outputs. The design of the RC filter is eased by the 4.7 kΩ resistor integrated into each I and Q output pin.

Phase-Locked Loop

The demodulators are driven by quadrature signals that are provided by a variable-frequency quadrature oscillator (VFQO), phase-locked to the reference frequency. This frequency is equal or double the frequency of the signal applied to Pin FREF. When the quadrature signals are at the IF, inphase and quadrature baseband outputs are generated at the I output (IRXP and IRXN) and Q output (QRXP and QRXN), respectively. The quadrature accuracy of the VFQO is typically within ±1° at 26 MHz. A simplified diagram of the FREF input is shown in Figure 32.

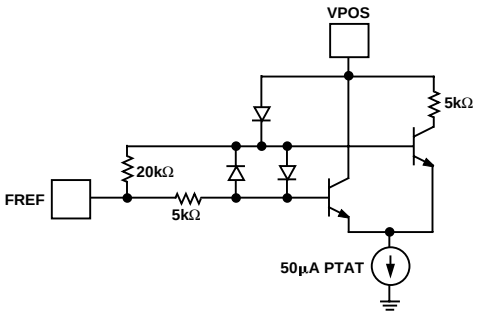


Figure 32. Simplified Schematic of the FREF Interface

The VFQO is controlled by the voltage between V_{POS} and FLTR. In normal operation, a series RC network, forming the PLL loop filter, is connected from FLTR to V_{POS}. The use of an integral sample-hold system ensures that the frequency-control voltage on Pin FLTR remains held during power-down, so reacquisition of the carrier occurs in less than 80 μs.

In practice, the probability of a phase mismatch at power-up is high, so the worst-case linear settling period to full lock needs to be considered in making filter choices. This is typically < 80 μs for a locking error of ±3° at an IF of 26 MHz. Note that the VFQO always provides quadrature between its own I and Q outputs, but the phasing between it and the reference carrier will swing around the final value during the PLL's settling time.

I and Q Transmit Modulator

The transmit modulator uses two standard mixer cells whose linear inputs are the differential voltages at the input Pins ITXP/ITXN and QTXP/QTXN, respectively and whose local oscillator inputs are derived from a divide-by-two cell, driven from the input applied to pins LOHI/LOLO. The outputs of the mixers are summed and converted to single-sided form. The output stage also filters the higher harmonics, minimizing the need for filtering before this signal is presented to the up-converter in a typical transmitter configuration.

The I and Q inputs are intended to be driven using a fully-differential drive (for example from an AD7015 or AD6421) and need to be biased to a common-mode dc level of 1.2 V, with a typical differential amplitude of ±1.028 V (that is, ±514 mV at each input). Some small variation in the drive conditions is allowable, but will result in nonoptimal performance. The minimum instantaneous input should not go below 0.6 V and the maximum voltage should not exceed 1.8 V using a 2.7 V supply (in general, VP – 0.9 V). The impedance at these inputs is several MΩ in parallel with approximately 1 pF; the bias currents flow out of the pins and are ~100 nA. These conditions permit the use of a high impedance low-pass filter if desired ahead of the modulator inputs.

The dc modulator output is at a constant dc level of 1.5 V, independent of temperature and supply voltage. It is designed to drive a 150 Ω load and should either be matched into a 50 Ω load, using a simple LC network, or padded to 150 Ω with a series 100 Ω resistor (Figure 33). The output is short-circuit-proof. The output modulated signal at pin MODO has a power of –16 dBm when driving a 50 Ω load with a 100 Ω series resistor, as shown in Figure 33. This power is specified at a carrier frequency of 272 MHz with a maximum dc differential signal applied to the I or Q channel while the other channel has no differential signal applied. The transmit modulator is enabled only when the TXPU input (Pin 39) is taken HI.

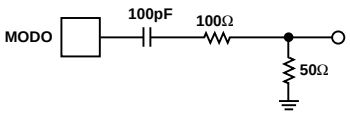


Figure 33. Output Impedance of Pin MODO Is Designed to Drive a 50 Ω Load with a 100 Ω Series Resistor

Local Oscillator Input
The Local Oscillator (LO) input port is differential and consists of two functionally identical pins, LOHI and LOLO. It accepts a signal of 200 mV p-p at a frequency between 200 MHz and 600 MHz. Inputs LOHI and LOLO are internally biased to the positive supply (Pin 3) through 500 Ω resistors. While not usually needed, these inputs may be driven through a simple matching network to lower the LO power required from a 50 Ω source. Single-sided drives are not recommended. The most noticeable effects will be degradation of phase balance and an increase in phase noise.

This signal is fed internally to a divider by two that generates the mixing signals for the receive mixer and the transmit modulator. In order to meet the phase and amplitude balance of the transmit quadrature modulator, as stated in the specification table, the duty cycle of the LO signal must be such that the second harmonic is at least 30 dBc below the fundamental.

I/Q Convention
The AD6432 is a complete IF subsystem. Although not a requirement for using the AD6432, most applications will use a high side LO injection on the receive mixer. The I and Q convention on the receive section is such that when a spectrum with I leading Q is presented to the input of the receive mixer and a high side LO is presented to the receive mixer, I still leads Q at the baseband output of the AD6432.

Likewise, the I and Q convention on the transmit section is such that when a spectrum with I leading Q is presented at the baseband input of the modulator, I still leads Q at the output of the modulator.

Auxiliary Op Amp
An auxiliary operational amplifier is available although it is important to remember that it is active only when TXPU is high. The positive and negative input terminals are PCAP and PCAM with PCAO being the output pin. The inputs are the bases of PNP transistors with a typical bias current of approximately 150 nA. The input offset voltage is typically < 4 mV and the open loop gain of the amplifier is 60 dB. The amplifier is unity gain stable with a –3 dB Bandwidth greater than 40 MHz. The input signal voltage range is from 0.1 V to V_{POS} – 2.1 V.

Bias System
The AD6432 operates from a single supply, V_{POS}, usually 3 V, at a typical supply current in receive mode of 13 mA at midgain and T_A = +25°C, corresponding to a power consumption of 39 mW. Any voltage from 2.7 V to 3.6 V may be used.

The bias system includes a fast-acting active high CMOS-compatible power-up switch, allowing the part to idle at less than 100 μA when disabled. Biasing is generally proportional-to-absolute temperature (PTAT) to ensure stable gain with temperature. Other special biasing techniques are used to ensure very accurate gain, stable over the full temperature range.

USING THE AD6432
In this section, we will focus on a few areas of special importance through the real life example of interfacing the AD6432 to the AD6421 Base Band converter. As is true of any wideband high gain components, great care is needed in PC board layout. The location of the particular grounding points must be considered with due regard for the possibility of unwanted signal coupling.

The high sensitivity of the AD6432 leads to the possibility that unwanted local EM signals may have an effect on the performance. During system development, carefully-shielded test assemblies should be used. The best solution is to use a fully enclosed box enclosing all components, with the minimum number of needed signal connectors (RF, LO, I and Q outputs) in miniature coax form.

Interfacing the AD6432 to the AD6421 Baseband Converter
The AD6421 Baseband Converter contains all the necessary elements to drive the AD6432.

Receive Interface
The interface between the two devices provides for quadrature I and Q channels that can be driven either differentially or in the single-ended configuration. Figure 35 shows the interface between the AD6432 and the AD6421 for the differential configuration. The respective pins (IRXP, IRXN, QRXP and QRXN) are dc coupled through 4.7 kΩ resistors, which are integrated within the AD6432. Balanced coupling may be used with a single 50 pF capacitor between the complementary signals as illustrated in Figure 35. This low-pass filter is the only external filter required to prevent aliasing of the baseband analog signal prior to sampling within the AD6421.

The AD6421 has an external autocalibration mode that can calibrate out any offsets resulting from the IF demodulation circuitry.

Transmit Interface
The corresponding transmit (ITXP, ITXN, QTXP and QTXN) pins of the AD6421 and AD6432 are directly connected as these have compatible bias levels for dc coupling. To meet the more stringent phase two filter mask requirements, an external low-pass filter may be required, depending on the filtering capabilities of the radio section. A passive second order low-pass filter network with a cutoff frequency to 600 kHz is suggested as shown in Figure 34. Resistor values should range from 1.5 kΩ–3.0 kΩ to minimize AD6432 offsets.

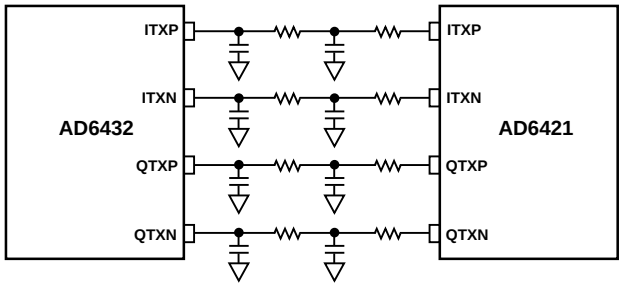


Figure 34. GSM Phase II Transmit Interface

Gain Control

The AD6432 contains a Gain TC Compensation circuit that provides a nominal 80 dB dynamic range of automatic gain control. The GAIN input pin of the gain circuit is driven by the AD6421 Automatic Gain Control DAC (AGCDAC), an integrated auxiliary DAC of the AD6421, controllable by the radio's digital processor. This connection should be made through a single pole RC to reduce high frequency noise into the gain control circuit. The values shown in Figure 35 provide a –3 dB point at approximately 1 MHz, sufficient for the gain control.

Gain control scaling is directly proportional to the reference voltage applied to Pin GREF and is independent of the power supply voltage. A nominal 1.2 V reference for GREF can be provided by the AD6421 through BREFOUT. BREFOUT is a buffered output version of BREFCAP reference. This reference output feature is enabled on the AD6421 by setting Bit 2 in control register BCRB (BCRB2). See AD6421 data sheet.

The V_{GAIN} input range for this control signal is 0.2 V– 2.4 V where gain is maximum at 0.2 V and falls off as V_{GAIN} is increased to 2.4 V. To avoid saturating the input to the baseband converter, the automatic gain control function of the receiver must limit the output signal swing of the AD6432 to ±1.2 V, the full signal range of the input.

Phase-Lock Loop Control

The AD6432 PLL/QVCO circuits require an external frequency reference for coherent modulation and demodulation of the baseband and IF signal. The external frequency reference control for the AD6432 PLL/QVCOs is typically generated through a 13 MHz voltage controlled temperature compensated crystal oscillator (VCTCXO). The control voltage for the VCTCXO is generated by an auxiliary DAC in the AD6421 designated as the Automatic Frequency Control DAC (AFCDAC). The PLL loop is closed through the radio's algorithm signal processor, which drives the AD6421 AFCDAC.

The AD6432 FREF pin provides the VCTCXO reference signal to the AD6432 RX quadrature VCO (QVCO) circuit. The AD6432 FREF input must be an ac coupled signal 200 mV p-p or greater. The reference for the UHF TX QVCO and RX IF down converter is synthesized from the VCTCXO output reference signal through an external frequency synthesizer and VCO. This UHF reference is an ac coupled input into AD6432 LOHI and LOLO pins.

An external series RC network connected between FLTR (Pin 29) and the VPOS supply pin provides the proper loop filter for the VCO/PLL as shown in Figure 35.

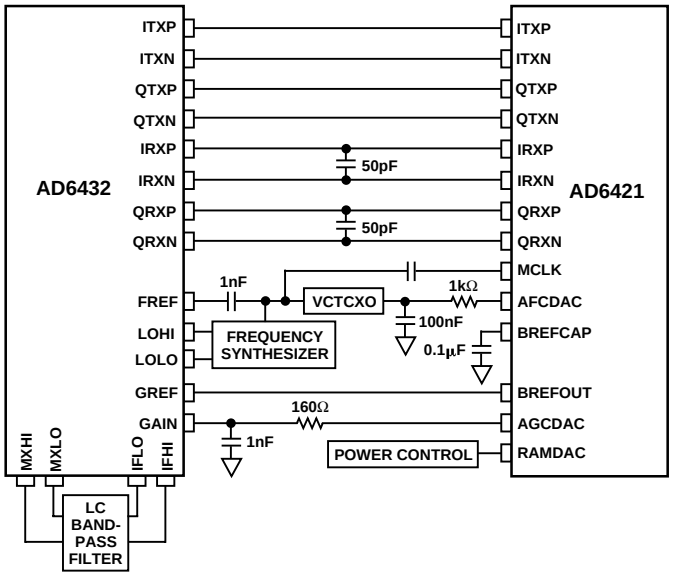


Figure 35. AD6432 to AD6421 Interface

Transmit Power Control

A general purpose amplifier is available on the AD6432, which may be useful as part of an automatic control circuit for the power amplifier. Open ended, this amplifier will swing full scale from rail to rail. It is recommended that this amplifier be connected in the unity feedback configuration when not being used by connecting PCAO to PGAM.

AD6432 EVALUATION BOARD

The AD6432 Evaluation Board is designed to enable measurements of key parameters on the AD6432 IFIC, a device that provides the complete transmit and receive IF signal processing, including I/Q modulation and demodulation, necessary to implement a digital wireless transceiver.

Many of the signal paths into and out of the AD6432 are differential, which is the preferred interface to and from single supply CODECS. To facilitate an interface to traditional lab equipment, the following interface circuitry is included on the board.

A 20-pin Berg strip for bias, gain and Inphase and Quadrature signal interface. End Launch SMA connectors for RF, LO, MODO and FREF signals and provisions for breaking out MXOP and IFHI with RF transformers.

A single-ended to differential RF transformer provides a balanced LO drive.

An onboard 1.2 V dc reference IC is provided for application to GREF.

Evaluation Board Description

This four layer board demonstrates both the transmit and receive functions of the AD6432. The top internal layer is a ground plane and the bottom internal layer is a strategically partitioned power plane with DUT power and bipolar support device power.

A 20-pin Berg strip connector provides the external power and dc signal interface, which includes power-up, gain and external reference bias options. The various high frequency IF, LO, TX Modulation output (MODO) and the Demodulator Reference (FREF) are brought in and out of the board via end-launch SMA connectors. Appropriate terminations are provided for each signal. Several hardware jumpers are provided for bias and IF selection options. Figure 36 shows the placement of the different connectors used on the evaluation board.

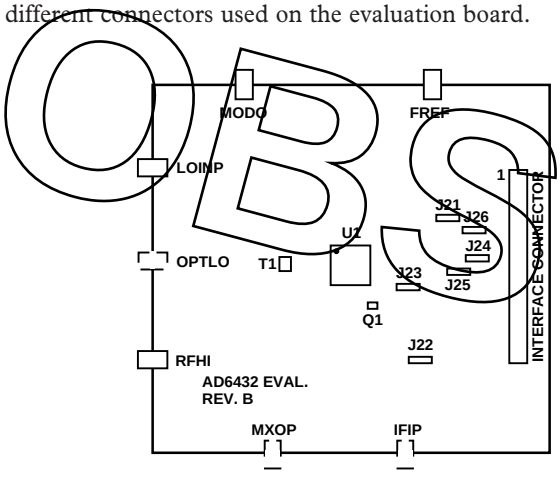


Figure 36. Evaluation Board Layout (Top View)

Note: MXOP, IFHI, OPTLO are optional SMA connectors not supplied with the evaluation board.

Interface Connector (Berg Strip) Pin Description

Building up a simple IDC connector/ribbon cable breakout to a vector board or box with banana plugs will facilitate testing. Figure 37 shows the signal's placement and Table II describes each signal.

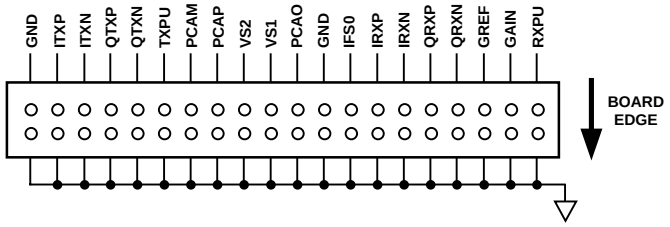


Figure 37. Evaluation Board Interface Connector

Table II. Connector Signal Description

Pin Name	Description
GND	Analog and Power Ground.
ITXP	I Channel Transmit Plus Modulation Input.
ITXN	I Channel Transmit Minus Modulation Input.
QTXP	Q Channel Transmit Plus Modulation Input.
QTXN	Q Channel Transmit Minus Input.
TXPU	Transmit Section Power-Up. This function is also jumper selectable with J21.
PCAM	Auxiliary Op Amp Minus Input.
PCAP	Auxiliary Op Amp Plus Input.
VS2	Power control op amp supply 2.7 V dc–3.6 V dc. The jumper, J26, connects VS1 and VS2 together.
VS1	AD6432 main supply 2.7 V dc–3.6 V dc.
PCAO	Auxiliary Op Amp Output.
IFS0	Selects IF Pin. This function is also jumper programmable with J25.
IRXP	I Channel Receive Plus Modulation Output.
IRXN	I Channel Receive Minus Modulation Output.
QRXP	Q Channel Receive Plus Modulation Output.
QRXN	Q Channel Receive Plus Modulation Output.
GREF	The AD6432 gain reference bias which is optimized for 1.2 V dc. This may be externally supplied; or by shorting J23, supplied directly from the AD1580 SOT-23 onboard, 1.2 V reference.
GAIN	Max RX gain occurs at 0.2 V dc. Minimum gain occurs at 2.4 V dc.
RXPU	Receive Section Power-Up. This function is also jumper selectable with J22.

Table III. SMA End-Launch Connectors

SMA	Connector Description
MODO	Transmit Modulator Output. This pin, which is designed to drive a 150 Ω filter, has been resistively matched (loss) onboard to drive a 50 Ω instrument such as a spectrum analyzer.
LOIP	Local Oscillator Input pin. This is actually fed with twice the LO frequency from a generator for both transmit and receive. The nominal LO level is –16 dBm (50 Ω).
OPTLO	Optional differential minus local oscillator input (transformer can be removed).
RFHI	RF input
MXOP	Mixer Output (optional output that may be converted to single ended output with an RF transformer).
IFHI	IF Input (optional single ended input that may be converted to differential with an RF transformer).
FREF	Frequency Reference for phase locked receive demodulator. The internal VCO frequency is equal to FREF in the 1X mode and equal to two times FREF in the 2X mode.

Power Requirements

The evaluation board uses two supplies, VS1 and VS2.

VS1—2.7 V dc–3.6 V dc, 13 mA typical. This is the main supply for the AD6432.

VS2—2.7 V dc–3.6 V dc, 2 mA typical. This is the supply for the on-chip op amp which is normally used in RF power control circuits.

The op amp is active only in the Transmit mode.

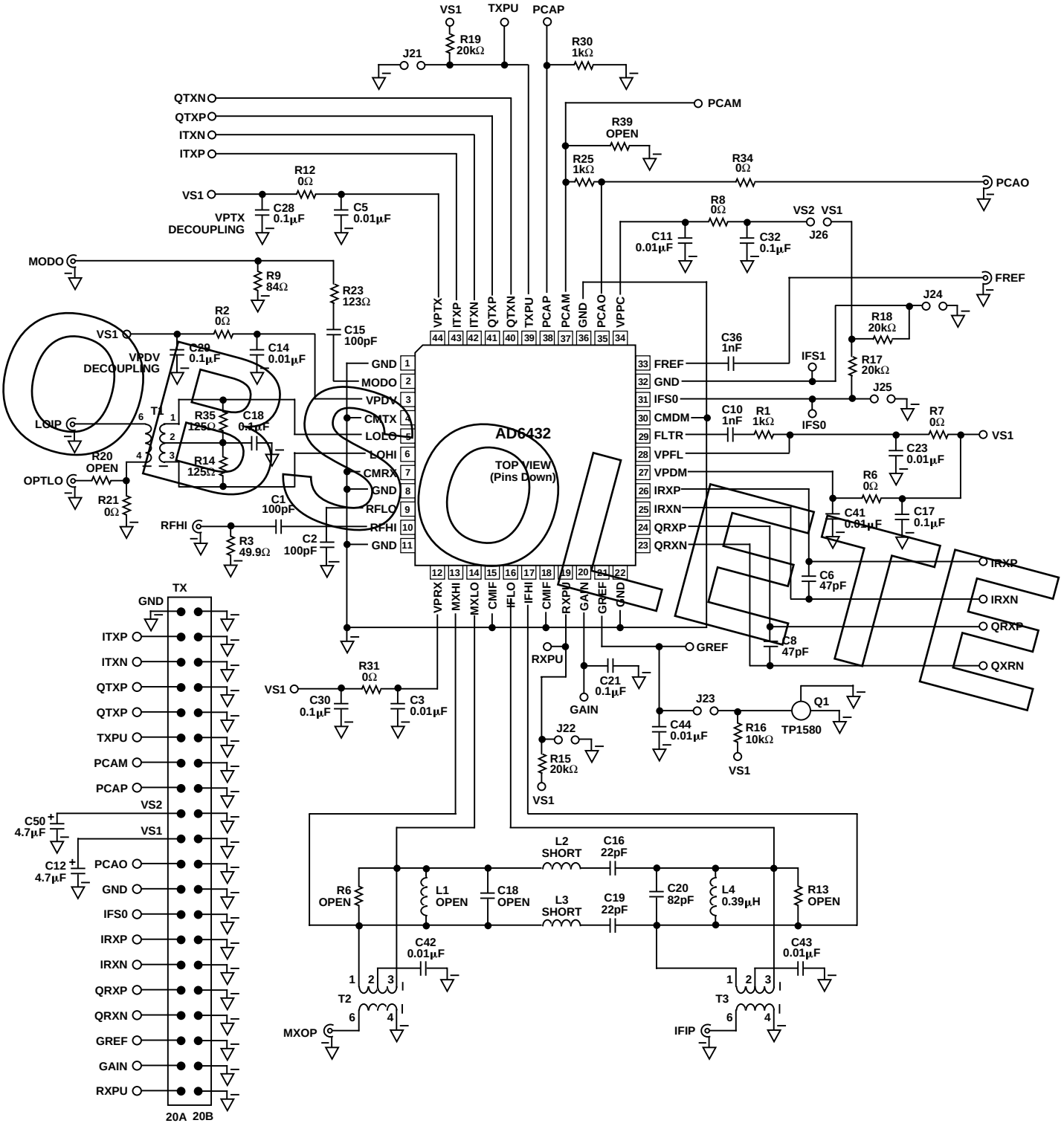
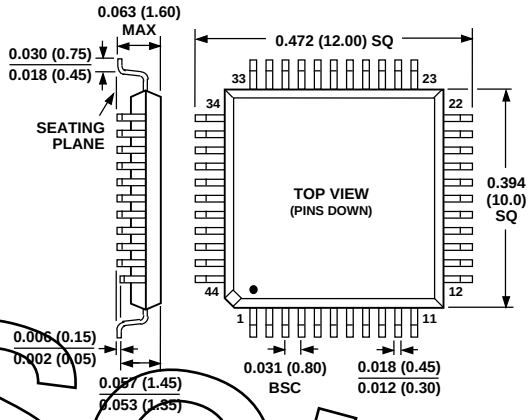


Figure 38. Evaluation Board Schematics

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Thin Quad Flatpack (TQFP)
(ST-44)



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